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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 29/49, 21/28, 21/336, 21/8238	A1	(11) International Publication Number: **WO 98/13880** (43) International Publication Date: 2 April 1998 (02.04.98)

(21) International Application Number: PCT/US97/04987

(22) International Filing Date: 25 March 1997 (25.03.97)

(30) Priority Data:
08/719,524 25 September 1996 (25.09.96) US

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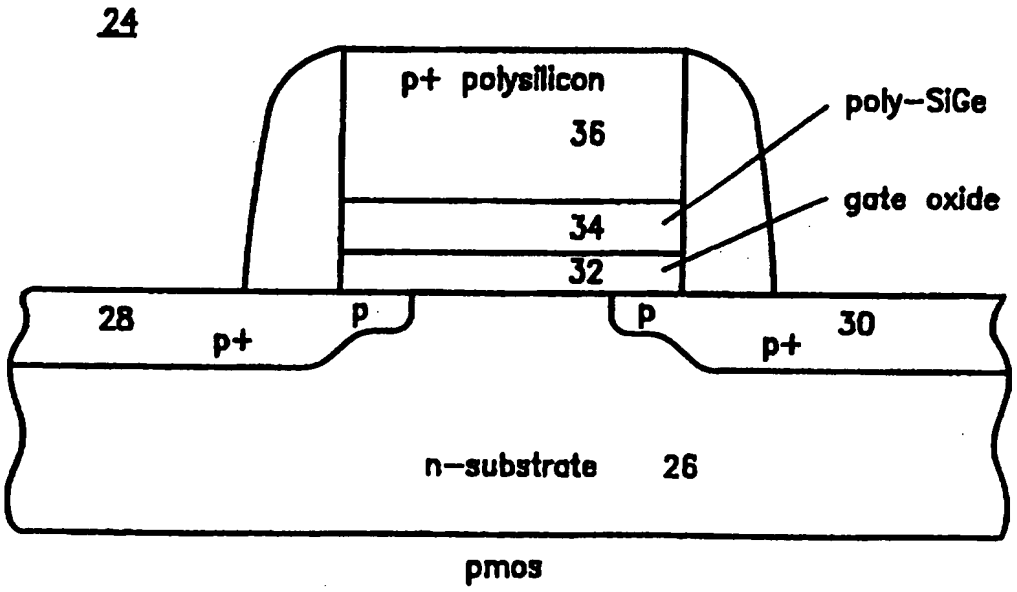
(81) Designated States: JP, KR, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: POLY–Si/POLY–SiGe GATE FOR CMOS DEVICES



(57) Abstract

A structure and a method of manufacturing the structure in which boron diffusion into a gate oxide layer is suppressed. The structure is formed on a semiconductor substrate and includes a gate oxide layer formed on the semiconductor substrate, a layer of doped or undoped poly–SiGe formed on the gate oxide layer. A polysilicon layer formed on the poly–SiGe layer. The polysilicon layer may be doped or undoped. If undoped, boron dopant ions are implanted in the polysilicon and heat diffused into the polysilicon layer and into the undoped poly–SiGe layer.

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POLY-Si/POLY-SiGe GATE FOR CMOS DEVICES

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to the manufacture of high performance semiconductor devices and, more particularly, to the manufacture of high performance sub-micron semiconductor devices and, even more particularly, to a gate structure to suppress boron penetration into thin gate oxides.

2. Discussion of the Related Art

The semiconductor industry is increasingly characterized by a growing trend toward fabricating larger and more complex circuits on a given semiconductor chip. This is being achieved by reducing the size of individual devices within the circuits and spacing the devices closer together. The reduction of the size of individual devices and the closer spacing brings about improved electrical performance.

For example, there is increasing interest in MOS integrated circuits in which the component devices have gate dimensions as small as 0.35 microns or less. Devices having such small dimensions suffer from certain problems that are not of serious concern when the gate dimensions are greater than about 1 micron. For example, the scaling rules that apply to these

small devices call for very thin gate oxide layers, typically equivalent to 30 - 80 Angstroms of silicon dioxide. Conventional gate oxide layers, which consist of thermally grown silicon dioxide, may be inadequate in several respects when they are made this thin. For example, such thin oxide layers tend to exhibit a high density of pinholes. These layers are also very permeable to boron which is used as a dopant for the polysilicon used as a gate material. As a result, for example, boron from a p^+ doped polysilicon gate electrode can readily penetrate the thin oxide layer and contaminate the underlying channel during subsequent, high-temperature processing.

Early MOS integrated circuits were built using PMOS technology, primarily because enhancement-mode MOSFETs with suitable V_t (threshold voltage) values could only be fabricated as p-channel devices using aluminum or n^+-doped polysilicon gates and uniform lightly doped n-substrates. This is because, at that time it was not possible to produce enhancement-mode n-channel MOSFETs using n^+-poly or Al gates on a uniform, lightly doped p-substrate because such structures exhibit a negative threshold voltage. However, with the advent of ion implantation it became possible to build NMOSFETs with positive V_ts by adjusting channel doping profiles. After this, enhancement-mode and depletion-mode NMOSFETs could then be fabricated with

little extra difficulty. Since n-channel transistors have greater drive current and hence speed, NMOS replaced PMOS as the dominant digital IC technology. However, when CMOS became the main technology for VLSI in the late 1980s, the need for enhancement-mode p-channel MOSFETs returned.

However, the fabrication of p-channel devices with short channels in CMOS present unique problems which arise from having to build both NMOS and PMOS devices on the same chip. The problems revolve around the choice of a doping type for the polysilicon gate electrode and the impact that this choice has on the threshold voltage and other characteristics of PMOS devices.

To achieve high drive current it is necessary to make the threshold voltage of a MOSFET as close to 0V as possible. When MOS IC technologies were initially being developed V_t values with a magnitude of about 1V were acceptable. However, in n-well CMOS technology, as well as in twin-well CMOS technology, the situation changes because in n-well CMOS technology the doping in the n-well is about 10x the doping in the substrate, making it at least $10^{16}/cm^3$. Twin-well CMOS technology has become the well-architecture technology of choice as the gate lengths decrease below about 1 micron. For 1 micron MOS devices, both p-channel and n-channel, the substrate doping density must be $2\text{-}3x10^{16}/cm^3$.

Therefore, the V_t values of PMOS devices made with n^+-poly gates in either n-well or twin-well CMOS technology will be at least -1.5V which is too large in magnitude. In addition, in PMOSFETs with a channel length less than 1 micron, punchthrough effects are more severe than in comparably sized NMOSFETs. This is primarily due to the inability to make p^+ source/drain junctions as shallow as n^+ junctions. To suppress such punchthrough current it is necessary to increase the n-doping in the substrate. This makes short-channel PMOS devices even more strongly enhancement mode, i.e., V_t is increased even more.

For optimal logic-gate performance the threshold voltages of the n-channel and p-channel devices in CMOS circuits should also have comparable magnitudes. In addition, to allow for maximum current-driving capability, they should be as small as possible. For example, for 5V CMOS technology, desirable threshold voltages are 0.6 to 0.8V for V_{Tn} and -0.6 to -0.8V for V_{Tp}.

The most common choice for the gate material has been heavily doped n-type polysilicon. For long-channel devices it has been possible to adjust both V_{Tn} and V_{Tp} with implants of boron into the channel. However, when n^+ poly is the gate electrode in a PMOS device, adjustment of V_{Tp} to -0.7V is not simple, especially when the channel is shrunk below about 1

microns. In addition, further shrinkage of the device requires the gate oxide to be thinner which makes the use of boron to adjust V_{Tp} in this type of device even less feasible since larger doses of boron are needed.

An alternative is to use p^+ polysilicon as the gate material for PMOS devices. This appears to be mandatory when the channel length becomes smaller than 0.5 μm.

In advanced CMOS technology having channel lengths below 0.50 μm, enhancement-mode surface-channel devices are desirable due to improved short-channel effect of these devices. The dual-poly (n^+-poly gate for NMOS and p^+-poly gate for PMOS) technology has been the trend in recent years, which produces surface-channel CMOS devices.

A major problem with p^+ polysilicon gates when a thin gate oxide is used is poor V_T process control in the PMOS devices, due to penetration of the boron into the gate oxide and, ever worse, into the silicon substrate. It has been shown that boron will penetrate gate oxides that are less than or equal to 12.5 nm thick during a 900 degree Centigrade, 30 minute post-implant anneal in N_2. This would imply that a lower process temperature needs to be used, however, if the process temperature is too low the boron implanted into the polysilicon will not be sufficiently redistributed and the polysilicon dopant concentration at the

polysilicon gate/gate-oxide interface could be less than the desired mid-$10^{19}/cm^3$ concentration level which would create V_T control problems in MOS devices. This produces the poly-depletion effect.

On the other hand, if the process temperature is too high or the anneal time is for too long a time, there will be boron penetration through the gate oxide. Boron penetration through thin gate oxide from the p^+ polysilicon in a dual gate (also known as twin gate) CMOS technology logic device results in threshold voltage V_T instability, a shift in the flat-band voltage V_{FB}, a degradation of channel mobility and subthreshold slope, a lower charge-to-breakdown Q_{BD} value, and an increase in oxide trapping centers for p-channel devices. Because of all these effects, boron penetration into the gate-oxide has become a major reliability concern for sub-halfmicron CMOS transistors due to the scaling of gate oxide.

The problem that is presented to process engineers in specifying process parameters is that for the p^+ polysilicon gate to act as a good conductor, so that drive currents are high, for example, it is necessary to have a uniformly heavily doped polysilicon gate.

The gate is doped by first ion implanting the dopant ions into the gate at a selected implant energy and then annealing at a selected temperature for a selected period of time to drive the dopant ions into

the polysilicon gate. Ideally, the dopant ions would be driven only until there is a uniform concentration profile across the polysilicon gate to the p+-polysilicon/gate-oxide interface and nothing beyond. However, the extent of the penetration of the dopant ions depends upon the process parameters, namely, the implant energy and dosage level at which the ions are implanted, the anneal temperature at which the ions are driven into the gate, and the period of time at which the anneal step is conducted. If one of these parameters is incorrect, the dopant ions will be driven either too far or not far enough. If the dopant ions are driven too far the problems, as discussed above occur. If the dopant ions are not driven far enough there is an area above the p+-polysilicon/gate-oxide interface that has a deficiency of dopant ions. This deficiency of dopant ions exhibits an effect known as the poly-depletion effect. Poly depletion decreases the effective gate capacitance of the device and degrades device current drive.

What is needed is a gate structure that will allow greater latitude for process engineers to specify process parameters such as heat treatment temperature and time, and that will decrease the extent of boron penetration at the gate/gate oxide interface in order to improve the reliability of the device and, at the same time, not decrease the performance of the device.

SUMMARY OF THE INVENTION

A gate structure and a method of manufacturing the structure in which boron diffusion into a gate oxide layer is suppressed. The structure includes a semiconductor substrate on which a gate oxide is formed. A boron diffusion suppression layer is formed on the gate oxide and can be either doped or undoped poly-SiGe. A doped or undoped polysilicon layer is formed on the poly-SiGe layer. The undoped polysilicon layer is implanted with dopant ions and heat treated to diffuse the dopant ions into the polysilicon layer and the poly-SiGe layer.

The present invention is better understood upon consideration of the detailed description below, in conjunction with the accompanying drawings. As will become readily apparent from the following description to those skilled in this art there is shown and described preferred embodiments of this invention simply by way of illustration of the mode best suited to carry out the invention. As it will be realized, the invention is capable of other different embodiments, and its several details are capable of modifications in various, obvious aspects all without departing from the scope of the invention. Accordingly, the drawings and descriptions will be regarded as illustrative in nature and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWING

The accompanying drawings incorporated in and forming a part of the specification, illustrate the present invention, and together with the detailed description serve to explain the principles of the invention. In the drawings:

Figure 1 is a diagram showing the structure as taught by the present invention in nmos.

Figure 2 is a diagram showing the structure as taught by the present invention in pmos.

Figure 3 shows boron concentration profiles in a polysilicon gate structure.

DETAILED DESCRIPTION

Referring now to **Figure 1**, there is shown an nmos semiconductor device **10** incorporating the present invention. The device **10** is formed on a p-silicon conductivity type substrate **12** which has two n+ regions **14** and **16** which are the drain and source regions, respectively, in the device **10**. A gate oxide region **18** is formed on the substrate **12** between the drain region **14** and the source region **16**. The thickness of the gate oxide region **18** is in the range of 20 - 70 Angstroms and the thickness selected depends on the dimensions of the overall device. For example, for 0.25 micron or smaller devices, a gate oxide thickness less than 60 Angstroms is necessary. For 0.1 micron devices, the

gate oxide thickness is required to be in the range of 20 - 40 Angstroms. The gate oxide is typically silicon dioxide, SiO_2. On the gate oxide region **18** there is a layer of poly-SiGe **20**. The poly-SiGe material is an alloy of silicon and germanium with the percentage of germanium in the range of 30-70%. The thickness of the poly-SiGe layer **20** is in the range of 10 - 200 Angstroms. The poly-SiGe layer **20** can be undoped or in-situ doped while being deposited. In one embodiment of the invention, undoped poly-SiGe is deposited on the gate oxide layer **18** and the polysilicon layer **22** is deposited on poly-SiGe layer **20**. The thickness of the polysilicon layer **22** is in the range of 500 - 3000 Angstroms. In the case in which the poly-SiGe layer **20** is deposited undoped the polysilicon layer **22** can be deposited undoped and boron implanted into the surface of the polysilicon layer **22** followed by a heat treatment to diffuse the boron ions into the polysilicon layer **22** and into the poly-SiGe layer **20**. In the case in which the poly-SiGe layer **20** is doped in-situ followed by the deposition of the polysilicon layer **22**, the polysilicon layer **22** can be deposited either in-situ doped or undoped as discussed above, that is, doped by implantation.

Referring now to **Figure 2** there is shown a pmos semiconductor device **24** incorporating the present invention. The device **24** is formed on an n- silicon

conductivity type substrate 26 which has two p+ regions 28 and 30 which are the drain and source regions, respectively, in the device 24. A gate oxide region 32 is formed on the substrate 26 between the drain region 28 and 30. The thickness of the gate oxide region 32 is in the range of 20 - 70 Angstroms and the thickness selected depends on dimensions of the overall device. For example, for 0.25 micron or smaller devices, a gate oxide thickness of less than 60 Angstroms is necessary. For 0.1 micron devices, the gate oxide thickness is required to be in the range of 30 - 40 Angstroms. The gate oxide is typically silicon dioxide, SiO_2.

On the gate oxide region 32 there is a layer of poly-SiGe 34. The poly-SiGe 34 material is an alloy of silicon and germanium with the percentage of germanium in the range of 30-70%. The thickness of poly-SiGe layer 34 is in the range of 10 - 200 Angstroms. The poly-SiGe layer 34 can be undoped or in-situ doped while being deposited. In one embodiment of the invention, undoped poly-SiGe is deposited on the gate oxide layer 32 and the polysilicon layer 36 is deposited on the poly-SiGe layer 34. The thickness of the polysilicon layer 36 is in the range of 500 - 3000 Angstroms. In the case in which the poly-SiGe layer 34 is deposited undoped, the polysilicon layer 36 can be deposited undoped and boron implanted into the surface

of the polysilicon layer 36 followed by a heat treatment to diffuse the boron ions into the polysilicon layer 36 and into the poly-SiGe layer 20. In the case where the poly-SiGe layer 34 is doped in situ followed by the deposition of the polysilicon layer 36, the polysilicon layer 36 can be deposited either in-situ doped or undoped as discussed above, that is, doped by implantation.

Referring now to Figure 3 there is shown boron concentration profiles at various stages of the manufacturing process. The boron concentration profiles are superimposed over a typical semiconductor device at 38. The relative concentration is given along the axis 40 and the depth into the structure coincides with the structure as shown along the axis 42. The typical structure 38, as taught by the present invention, is formed on a silicon substrate 44 of a selected conductivity type, a gate oxide layer 46, typically made of SiO_2, a poly-SiGe layer 48, and a polysilicon layer 50. The curve 52 represents the boron ion concentration profile as implanted. As can be appreciated, the highest boron ion concentration immediately after implant is in the polysilicon layer 50 with decreasing concentration in the poly-SiGe layer 48. Ideally, there is no boron ion penetration into the SiO_2 layer 46 through the interface 54. The curve 56 represents the boron ion concentration profile after

heat treatment which is done to drive a higher concentration of boron ions into the poly-SiGe layer **48**. The ideal concentration profile is for the curve **56** to be uniform across the polysilicon layer **50** and the poly-SiGe layer **48** with no boron ion concentration indicated across the interface **54** into the gate oxide layer **46**. However, there is penetration of boron ion into the gate oxide layer **46** as indicated by the portion of curve **56** indicated at **58** which represents the situation when there is no poly-SiGe layer **48**, that is, if polysilicon layer **50** extends to the gate oxide layer **46**. In contrast, with the poly-SiGe layer **48** in the device, the boron ion concentration profile curve **56** follows the curve **60** which shows a decreased concentration in the poly-SiGe layer **48** and a much less concentration beyond the interface **54** indicated by **61**. The decreased concentration of boron ions in the oxide layer **46** improves oxide reliability, and the suppressed diffusion into the gate oxide layer **46** prevents the boron ions from reaching the substrate **44** which improves pmos threshold stability.

The advantages of using the poly-SiGe layer **20** in the nmos device shown in **Figure 1** and the poly-SiGe layer **34** in the pmos device shown in **Figure 2** are as follows:

1. Boron doped poly-SiGe provides a symmetric V_t for nmos and pmos. This provides for single

polysilicon devices which have similar surface channel characteristics.

2. No V_t implant is required. Low surface doping leads to high mobility and high current drive.

3. Since poly-SiGe is a better barrier to boron diffusion than conventional polysilicon process engineers have greater latitude in developing processes to suppress boron penetration to the gate oxide.

4. Because conventional polysilicon is stacked onto the poly-SiGe layer which is very thin compared to polysilicon, all of the process parameters developed for polysilicon can be used in the remaining process steps. These process parameters include standard etching, lithography, silicidation, and oxidation properties, etc.

5. Both implanted boron polysilicon and in-situ boron doped polysilicon can be used.

6. Both undoped and in-situ doped poly-SiGe can be used.

The foregoing description of the preferred embodiments of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Obvious modifications or variations are possible in light of the above teachings. The embodiments were chosen and described to provide the best illustration of the principles of

the invention and its practical application to thereby enable one of ordinary skill in the art to utilize the invention in various embodiments and with various modifications suited to the particular use contemplated. All such modifications and variations are within the scope of the invention as determined by the appended claims when interpreted in accordance with the breadth to which they are fairly, legally, and equitably entitled.

CLAIMS

What I claim is:

1. A semiconductor device, comprising:

a semiconductor substrate of a first conductivity type;

a gate oxide layer formed on said semiconductor substrate; and

a boron diffusion suppression layer formed on said gate oxide layer.

2. The semiconductor device of Claim 1, wherein said boron diffusion suppression layer comprises a layer of poly-SiGe.

3. The semiconductor device of Claim 2, wherein said layer of poly-SiGe is doped.

4. The semiconductor device of Claim 2, wherein said layer of poly-SiGe is undoped.

5. The semiconductor device of Claim 3, further comprising a polysilicon layer formed on said boron diffusion suppression layer.

6. The semiconductor device of Claim 4, further comprising a polysilicon layer formed on said boron diffusion suppression layer.

7. The semiconductor device of Claim 6, further comprising a doped polysilicon layer.

8. The semiconductor device of Claim 7, further comprising heat diffused dopant ions in said polysilicon layer.

9. The semiconductor device of Claim 8, further comprising heat diffused dopant ions in said boron diffusion suppression layer.

10. The semiconductor device of Claim 5, wherein said polysilicon layer is doped.

11. A method of manufacturing a semiconductor device, comprising the steps of:

forming a gate oxide layer on a semiconductor substrate of a first conductivity type; and

forming a boron diffusion suppression layer on said gate oxide layer.

12. The method of Claim 11, wherein said step of forming a boron diffusion suppression layer on said gate oxide layer is accomplished by a step of forming a layer of poly-SiGe on said gate oxide layer.

13. The method of Claim 12, wherein said step of

forming a layer of poly-SiGe on said gate oxide layer is accomplished by the step of forming a layer of doped poly-SiGe on said gate oxide layer.

14. The method of Claim 12, wherein said step of forming a layer of poly-SiGe on said gate oxide layer is accomplished by the step of forming a layer of undoped poly-SiGe on said oxide layer.

15. The method of Claim 13, further comprising the step of forming a polysilicon layer on said boron diffusion suppression layer.

16. The method of Claim 14, further comprising the step of forming a polysilicon layer on said boron diffusion suppression layer.

17. The method of Claim 16, further comprising the step of doping the polysilicon layer.

18. The method of Claim 17, further comprising the step of heat diffusing said implanted dopant ions into said polysilicon layer.

19. The method of Claim 18, further comprising the step of heat diffusing said dopant ions into said boron diffusion suppression layer.

20. The method of Claim 15, wherein said step of forming a polysilicon layer on said boron diffusion suppression layer is accomplished by forming a layer of doped polysilicon on said gate oxide layer.

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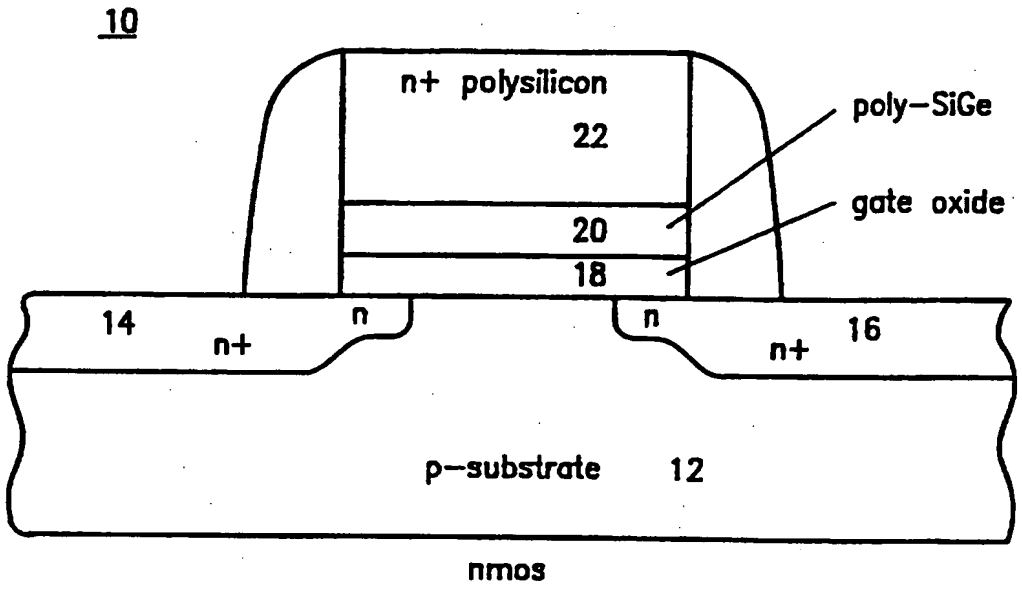

FIG. 1

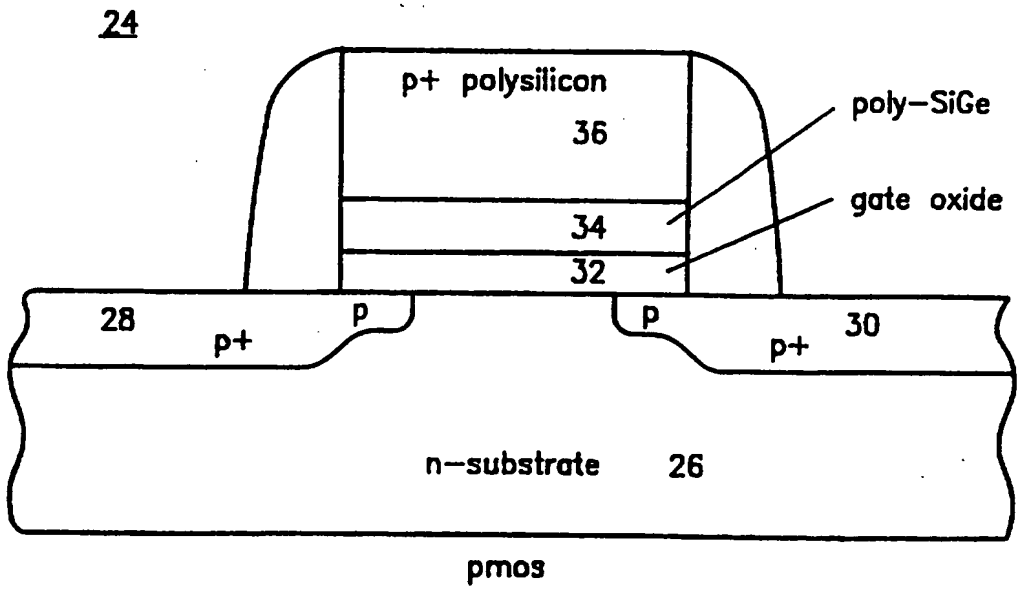

FIG. 2

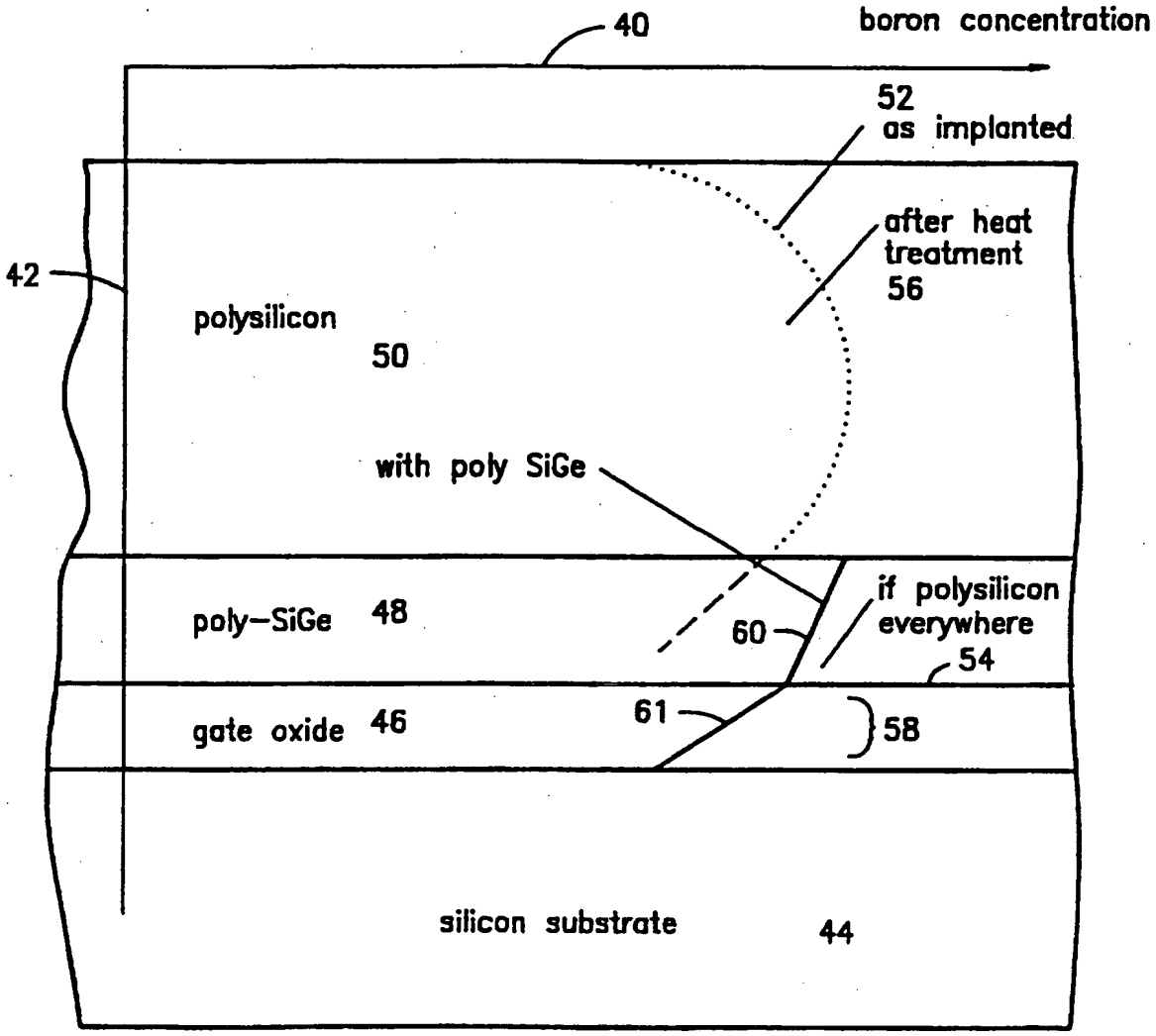

FIG. 3

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 97/04987

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L29/49 H01L21/28 H01L21/336 H01L21/8238

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PROCEEDINGS OF THE INTERNATIONAL ELECTRON DEVICES MEETING, WASHINGTON, DEC. 5 - 8, 1993, 5 December 1993, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 727-730, XP000481716 KISTLER N ET AL: "SYMMETRIC CMOS IN FULLY-DEPLETED SILICON-ON-INSULATOR USING P+- POLYCRYSTALLINE SI-GE GATE ELECTRODES" see page 728, left-hand column; figure 4 ---	1-3,5, 10-12, 14,16-19
X Y	PATENT ABSTRACTS OF JAPAN vol. 017, no. 401 (E-1404), 27 July 1993 & JP 05 075136 A (OKI ELECTRIC IND CO LTD), 26 March 1993, see abstract; figures 1,2,5,6 --- -/--	1,2,4,6, 7,11,12, 14,16,17 3,5, 8-10,15, 18-20

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
11 July 1997	23 -07- 1997
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Authorized officer Gélébart, J

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 97/04987

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	1995 SYMPOSIUM ON VLSI TECHNOLOGY. DIGEST OF TECHNICAL PAPERS, KYOTO, JUNE 6 - 8, 1995, no. SYMP. 15, 6 June 1995, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, page 121/122 XP000580849 SUN S C ET AL: "RAPID THERMAL CHEMICAL VAPOR DEPOSITION OF IN-SITU NITROGEN-DOPED POLYSILICON FOR DUAL GATE CMOS"	1,12
Y	see page 121; figure 1	3,5, 8-10,18, 19

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Y	see page 253 - page 254	15,20

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